CLAIMS

We claim:

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1. A method of forming an active area surrounded with an insulating area in a semiconductor substrate, comprising the steps of:

a) forming in the substrate a trench surrounding an active area;

b) filling the trench with an insulating material to form an edge extending beyond a surface of the substrate at a periphery of the active area;

c) forming a spacer at a periphery of said edge; and

d) implanting a dopant in the active area, whereby the implantation in a area located under the spacer is less deep than in the rest of the active area.

2. The method of claim 1, wherein the spacer has a substantially vertical edge or has a bell shape, with a thickness that thins down as the distance from said edge increases.

3. The method of claim 1, wherein the implantation step is followed by a step of removing the spacer.

4. The method of claim 3, wherein the step of removing the spacer is preceded or followed by a step of implantation of another active area with a dopant of another conductivity type than that of the dopant used at step d).

5. The method of claim 1, wherein a step of forming, at the surface of the active area, a protective coating between the trench filling step and spacer forming step c).

6. The method of claim 5, wherein the protective coating results from the thermal growth of a thin silicon oxide layer at the surface of the substrate.

7. The method of claim 1, wherein the spacer is made of silicon nitride.

8. The method of claim 1, wherein the spacer is made of polysilicon.

9. A MOS transistor, comprising a doped effective channel area adjacent to trench filled with an insulating material, wherein the channel area includes a first portion in contact with the insulating material layer and a second portion spaced from the insulating material, the second portion being more deeply doped than the first portion.

10. The MOS transistor of claim 9 wherein the channel area is part of a semiconductor substrate and the insulating area extends into the substrate and has a lower surface below the surface of the channel area.

11. The MOS transistor of claim 10 wherein the channel area includes:

a first well region that extends into the substrate to a level below the lower surface of the insulating area; and

a second well region that extends into the first well region, the second well region extending from the surface of the channel region further in the second portion than in the first portion.

12. The MOS transistor of claim 11 wherein the substrate has a first conductivity type and the well regions each have a second conductivity type opposite to the first conductivity type.

13. A method of forming a doped active area in a semiconductor substrate, comprising:

forming first and second insulation areas on a surface of the substrate, the first and second insulation areas being spaced apart from each other and thereby defining a substrate region of the substrate between the first and second insulation areas, the substrate region having

a first peripheral portion immediately adjacent to the first insulation area and a central portion spaced apart from the first insulation area;

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forming a first spacer adjacent to the first insulation area and above the first peripheral portion of the substrate region; and

performing, after forming the first spacer, a first dopant implant into the substrate region to create the doped active area, the first spacer acting as a mask to allow dopants to extend deeper into the central portion that into the first peripheral portion.

14. The method of claim 13 wherein the substrate region has a second peripheral portion immediately adjacent to the second insulation area, the method further comprising forming a second spacer adjacent to the second insulation area and above the second peripheral portion of the substrate region, wherein performing the first dopant implant is executed after forming the second spacer, the first spacer acting as a mask to allow dopants to extend deeper into the central portion that into the second peripheral portion

15. The method of claim 13, further comprising:

forming in the substrate first and second trenches on opposite sides of the substrate region, wherein forming the first and second insulation areas includes filling the trenches with insulating material and extending the insulating material to a level above a surface of the substrate region.

16. The method of claim 15 wherein the first dopant implant forms a first well that extends into the substrate region to a first level and the first and second trenches extend into the substrate to a second level, the method further comprising performing a second dopant implant into the substrate region, thereby forming a second well that extends into the substrate region to the second level.

17. The method of claim 13, wherein the first spacer has a bell shape with a thickness that thins down as the distance from the first insulation area increases.

18. The method of claim 13, further comprising:

removing the first spacer after performing the first dopant implant; and

depositing a first conductive layer on the substrate region.

19. The method of claim 13, further comprising forming a protective coating directly on the substrate region before forming the first spacer, the first spacer being formed on the protective coating.

20. The method of claim 13 wherein the first spacer is made of silicon nitride.